

In the claims:

This listing of claims will replace all prior versions and listings of claims in the application:

1 1-10. (canceled).

1 11. (currently amended) The automated method of claim 19 determining the initial delay values
2 based on wherein the preferred gain considerations of the cells including is determined using a
3 continuous buffering assumption.

1 12. (previously presented) The automated method of claim 19 wherein said initial delay values
2 are determined during library analysis.

1 13-18. (canceled).

1 19. (currently amended) An automated method for designing an integrated circuit layout with a
2 computer, comprising:

3 selecting cells from a cell library to implement a circuit path;

4 prior to assignment of wire loads based on an initial placement of the circuit path,

5 determining initial delay values for the selected cells ~~based on corresponding preferred gains of~~
6 ~~the selected cells;~~

7 prior to the assignment of wire loads based on the initial placement of the circuit path,

8 determining an adjusted initial delay value for at least one of the selected cells by performing at
9 least one of:

10 compressing the initial delay value of at least one of the selected cells to meet delay

11 constraints for the circuit path, and

12 stretching the initial delay value of at least one of the selected cells to reduce slack in
13 the circuit path;

14 performing ~~[[a]]~~ the initial placement of the selected cells for the circuit path, ~~including~~
15 ~~assigning and the assignment of~~ wire loads to the selected cells based on the initial placement;

16 adjusting size or area of one or more of the selected cells during or after the initial
17 placement ~~in response to the assigned wire loads~~, to maintain the initial delay value or the
18 adjusted initial delay value for the corresponding selected cells; and
19 routing the selected cells for the circuit path.

1 20. (currently amended) The automated method of claim 19, including prior to the initial
2 placement, inserting a buffer in the circuit path when there is available slack in the circuit path.

1 21. (currently amended) The automated method of claim 20, including prior to the initial
2 placement, determining net weight values for the selected cells, the net weight values
3 representing sensitivity of total area of a circuit design to load on the corresponding cell, and
4 determining whether to insert a buffer on the output of a given cell in the selected cells using the
5 net weight value of the given cell.

1 22. (new) An automated method for designing an integrated circuit layout with a computer,
2 comprising:
3 selecting cells from a cell library to implement a circuit path;
4 prior to assignment of wire loads based on an initial placement of the circuit path,
5 determining initial delay values for the selected cells;
6 prior to the assignment of wire loads based on the initial placement of the circuit path,
7 determining an adjusted initial delay value for at least one of the selected cells by performing at
8 least one of:
9 compressing the initial delay value of at least one of the selected cells to meet delay
10 constraints for the circuit path, and
11 stretching the initial delay value of at least one of the selected cells to reduce slack in
12 the circuit path; and
13 performing the initial placement of the selected cells for the circuit path, and the
14 assignment of wire loads to the selected cells based on the initial placement;
15 adjusting size or area of one or more of the selected cells during or after the initial
16 placement to maintain the initial delay value or the adjusted initial delay value for the
17 corresponding selected cells;

18 routing the selected cells for the circuit path; and further including
19 determining net weight values for the selected cells, the net weight values representing
20 sensitivity of total area of a circuit design to load on the corresponding cell, and prior to
21 placement of the circuit path, determining whether to insert a buffer on the output of a given cell
22 in the selected cells using the net weight value of the given cell, and inserting a buffer in the
23 circuit path when there is available slack in the circuit path.

1 23. (new) The automated method of claim 19 wherein said initial delay values are determined
2 based on a typical load value determined using gain considerations.

1 24. (new) The automated method of claim 22 wherein said initial delay values are determined
2 based on a typical load value determined using gain considerations.

///